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United States Patent

[19]

Williams et al.

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[54] **CHECK BIT CODE CIRCUIT FOR SIMULTANEOUS SINGLE BIT ERROR CORRECTION AND BURST ERROR DETECTION**

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[58] Field of Search 371/37.1, 37.4, 371/37.6, 37.9, 38.1, 39.1, 40.1, 40.4

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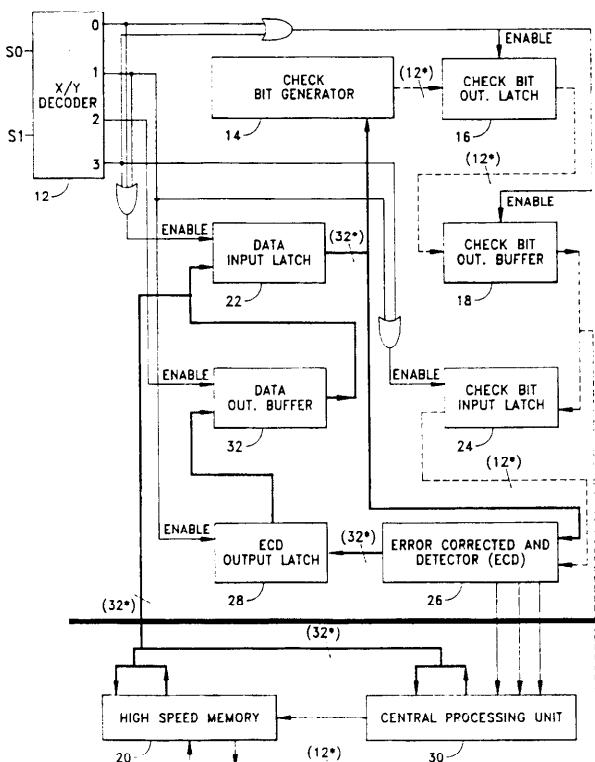
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[57] **ABSTRACT**

A system for correcting a single bit error and detecting burst errors is provided. A check bit generator generates partition check bits and burst check bits based on a H-parity matrix data regeneration scheme which provides an a single error correction and multiple bit error detection code which is linear and has the property of self orthogonality within a subclass of self orthogonal codes exclusive of Latin square codes. These check bits provide two independent sources for ascertaining the correct value for any given data bit. An error corrector and detector takes as input the data bits and check bits and provides a corrected data bit output as well as a set of error status lines. The error corrector and detector consists of Error Corrector, error corrector/detector and Error Status modules. The Error Corrector and error corrector/detector modules run in parallel providing a high speed Error Correction and Detection implementation, and providing a simplicity of logic structure compatible with application specific integrated circuit (ASIC) design and production processes.

7 Claims, 9 Drawing Sheets



(n*) FOR APPLICATIONS IN WHICH p=32

CONTROL
DATA
CHECK BITS